

Measurements for industrial sustainability and environmental safety

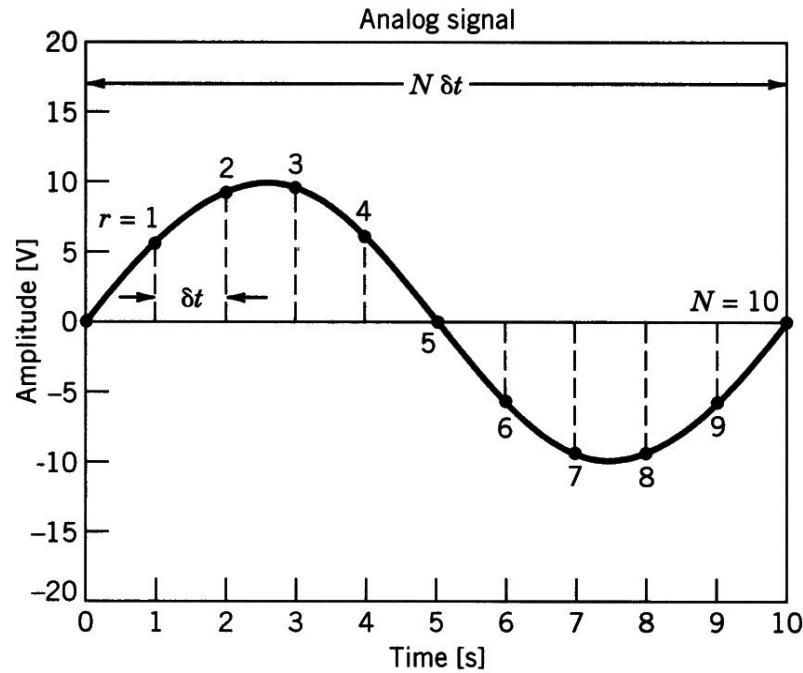
PART II Lesson 8

A.Y. 2026-27
Ludovica Apa



Analog to Digital (A/D) Conversion:

Electronic and Digital Counters are fundamental devices for Analog to Digital and Digital to Analog Conversion



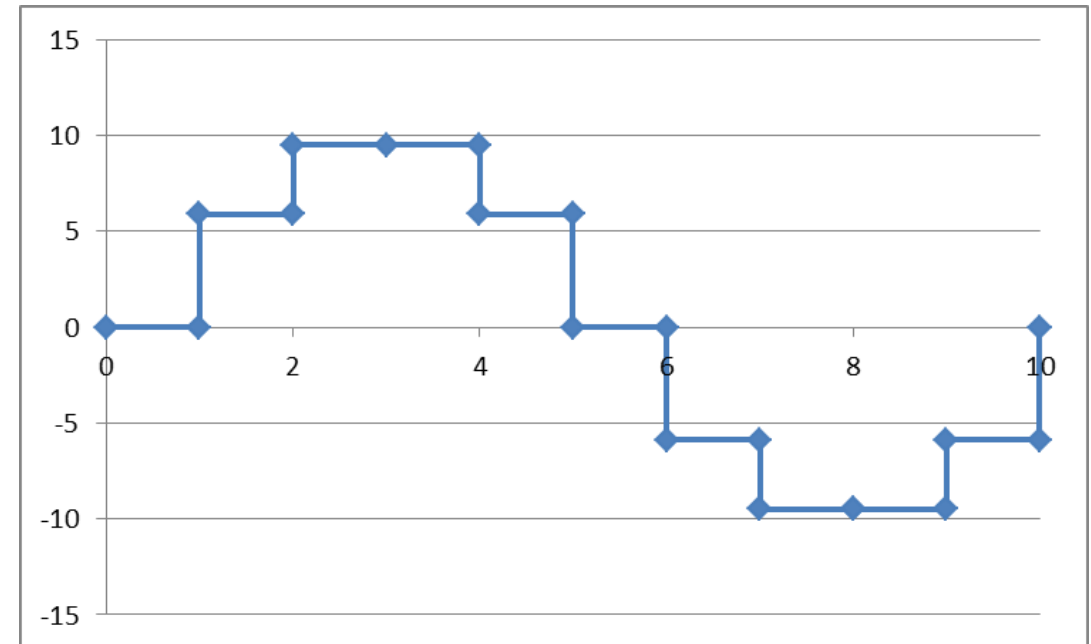
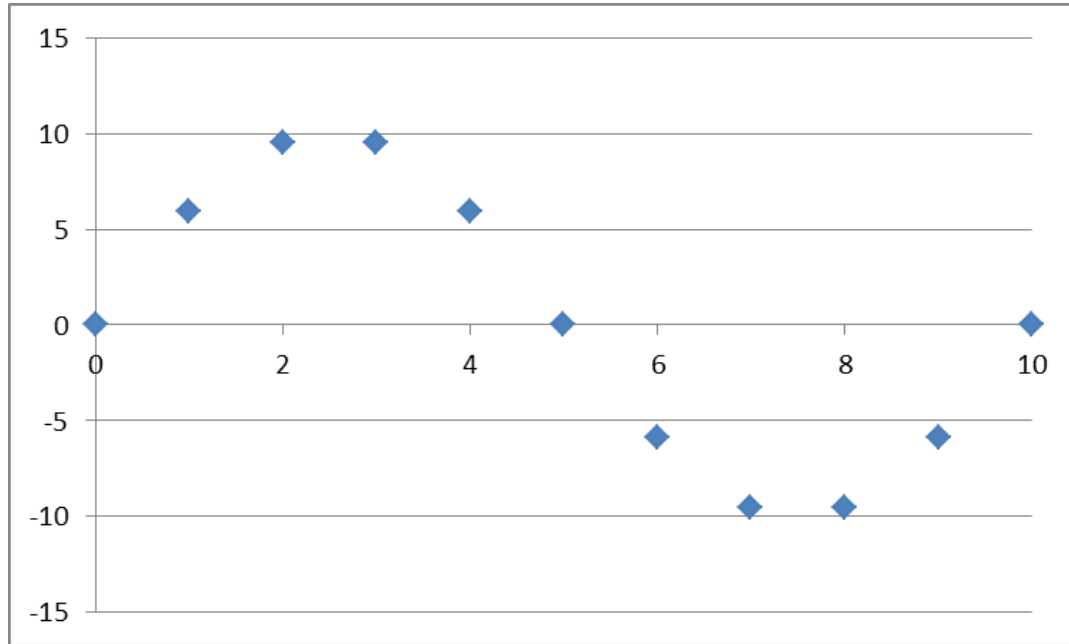
Discrete time signal	
$\{y(r\delta t)\}$	
r	Discrete data
0	0
1	5.9
2	9.5
3	9.5
4	5.9
5	0
6	-5.9
7	-9.5
8	-9.5
9	-5.9
10	0

Analog and discrete representations of a time-varying signal.

$V(t)$ → **A/D Converter** → 011001

- **Sampling a signal** means to “extract”, from the analog continuous voltage signal, a certain number of values (the **samples**), measured at a regular time distance (the **sampling period**) !
- *Sampling a signal* is always a *loss of information* !
- The inverse of the sampling period is the **sampling frequency** :
$$f_c = 1/T_c$$
- *If the sampling frequency is not “chosen carefully” the information of the analog measured signal can be completely spoiled !*
- The “sampling” procedure is done by special electronic devices called **A/D Converters**

Sampling a signal ...

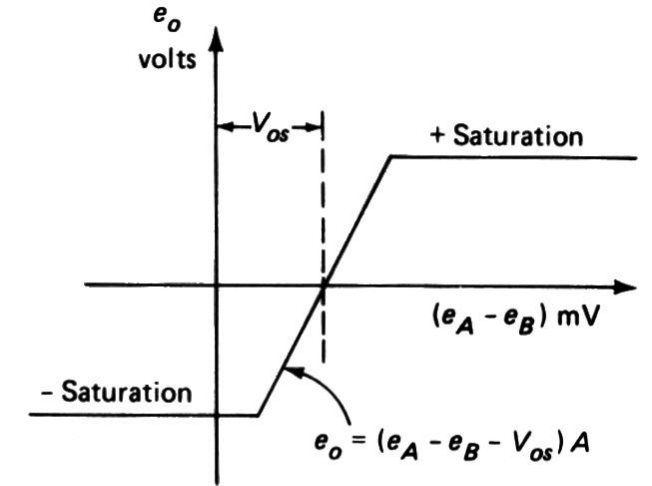
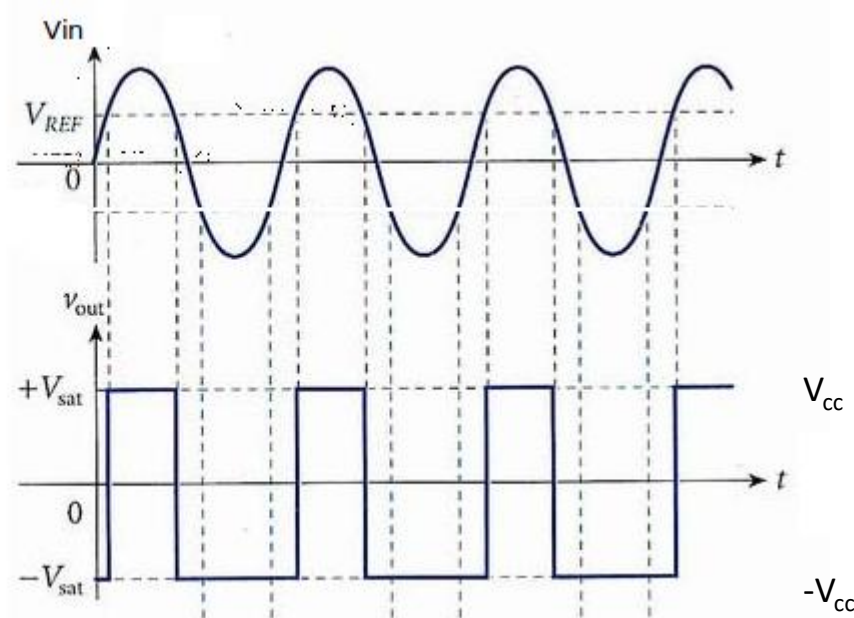
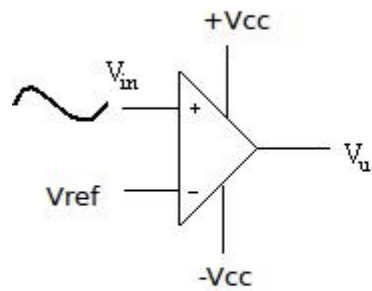


AO as a comparator:

if V_{ref} is connected to $-$, we have the non-inverting comparator (V_{in})

if V_{ref} is connected to $+$, we have the inverting comparator (V_{in})

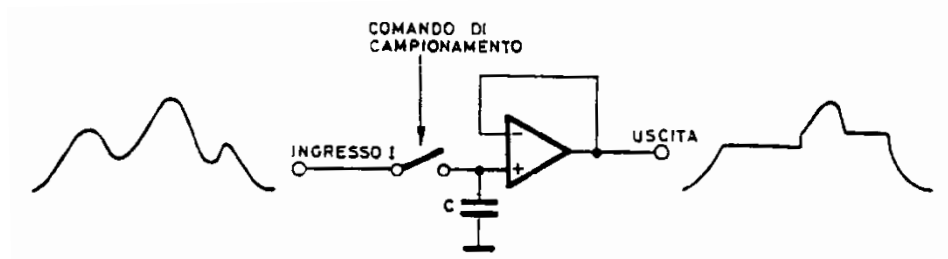
$$V_{\text{OUT}} = A(V_+ - V_-)$$



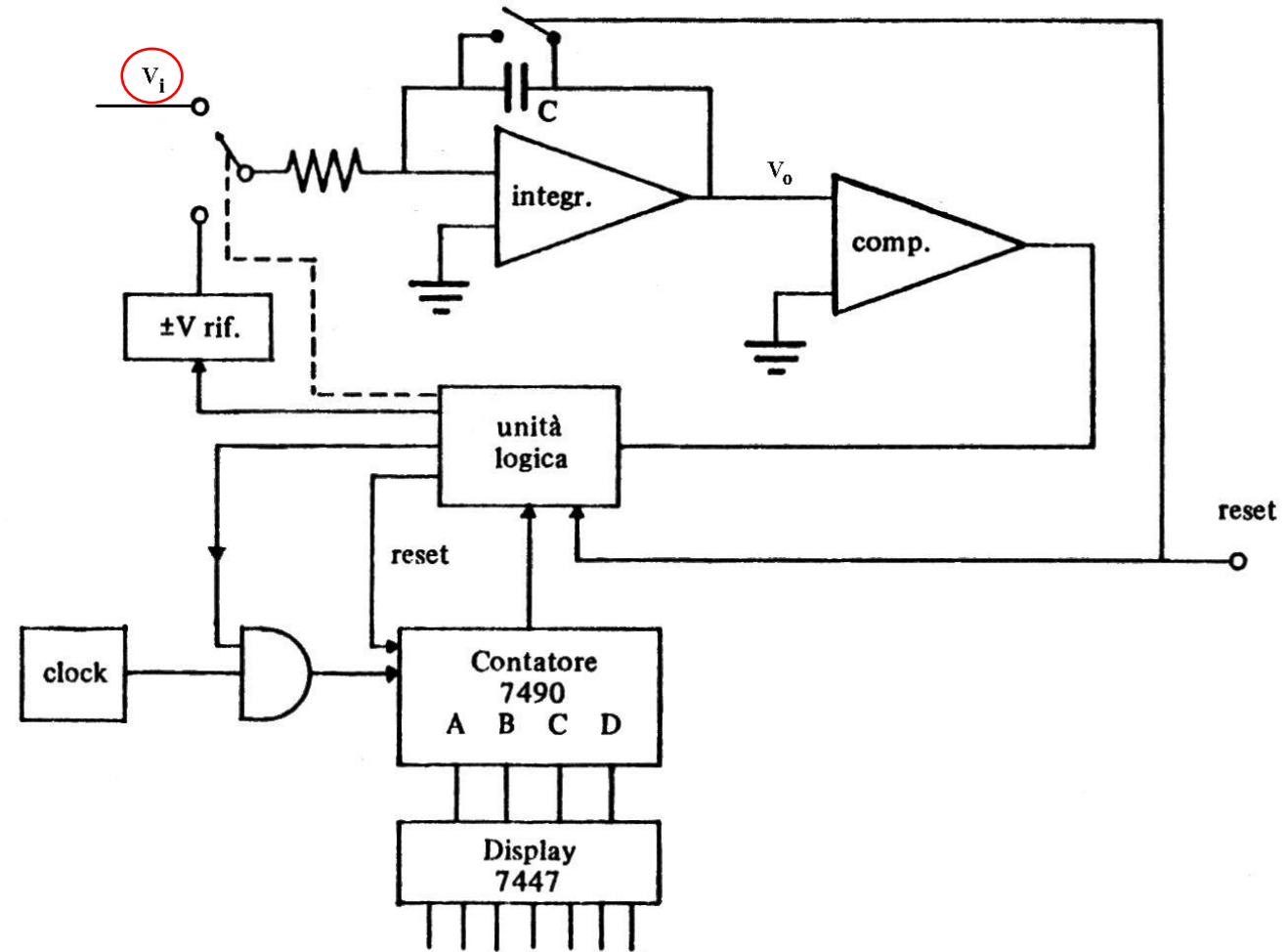
Today there are many different types of *A/D converters* employed in so many *appliances of consumer electronics*. We will study the three most important ***A/D converters for measurement instruments*** :

The ***integrating converter*** or ***voltage to time converter*** is the device which equips all the bench digital voltmeters in the laboratory !

The analog signal v_i must be kept constant for all the time of the conversion; this task is performed by an external device the ***sample and hold circuit*** :



- 1 integrator
- 1 comparator
- 1 reference voltage generator
- a circuit for time measurement

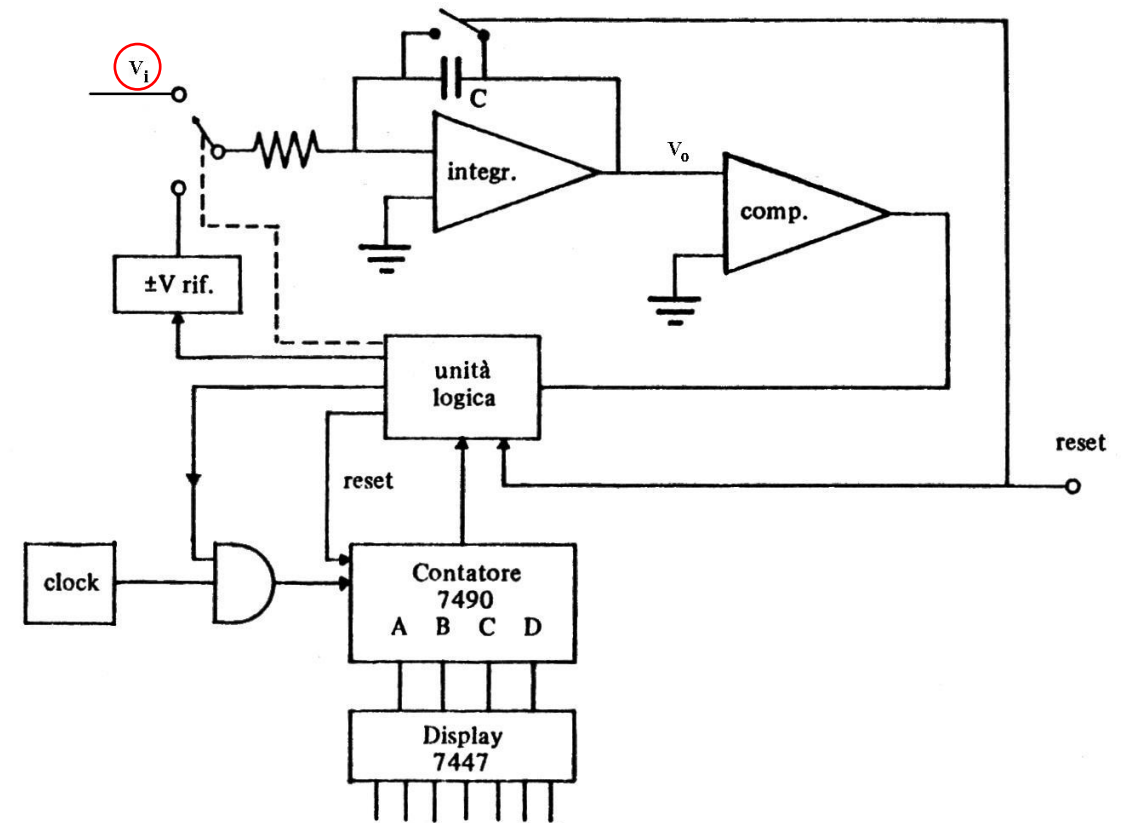


The logic unit connects the constant input signal v_i to the integrator for a fixed time T , the output voltage v_o will be:

$$V_o = -\frac{1}{CR} \int_0^T V_i dt = -\frac{V_i}{CR} \int_0^T dt = -\frac{V_i \cdot T}{CR} = -\frac{T}{CR} \cdot V_i$$

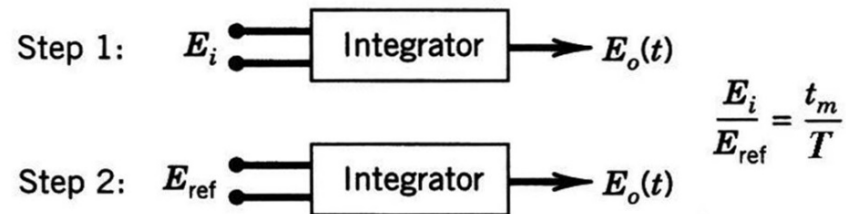
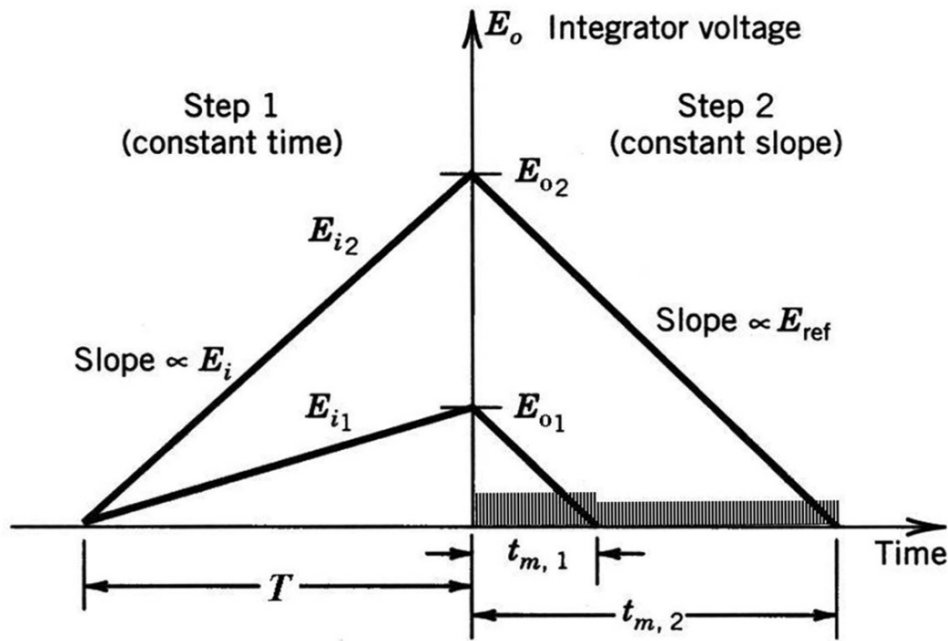
After the fixed time T , the logic unit switches the integrator input to an internal signal $-v_r$, whose value has always the *opposite sign* of the input signal.

Both signals v_i and $-v_r$ are constant and produce two ramps at the integrator output v_o ...



The integrator output voltage v_o at time T reflects the charge accumulated by the capacitor C during that time, which is also the charge the same capacitor releases during the time t_m of the descending ramp:

$$Q = V_i \cdot T = -V_r \cdot t$$



Therefore: $V_i = -\frac{V_r}{T} \cdot t$, the device characteristic curve !

Because v_r and T are constant for every input signal v_i , **the signal v_i is simply proportional to the measured time t_m** which, in fact, is different for each input voltage v_{i1} , v_{i2} , ...

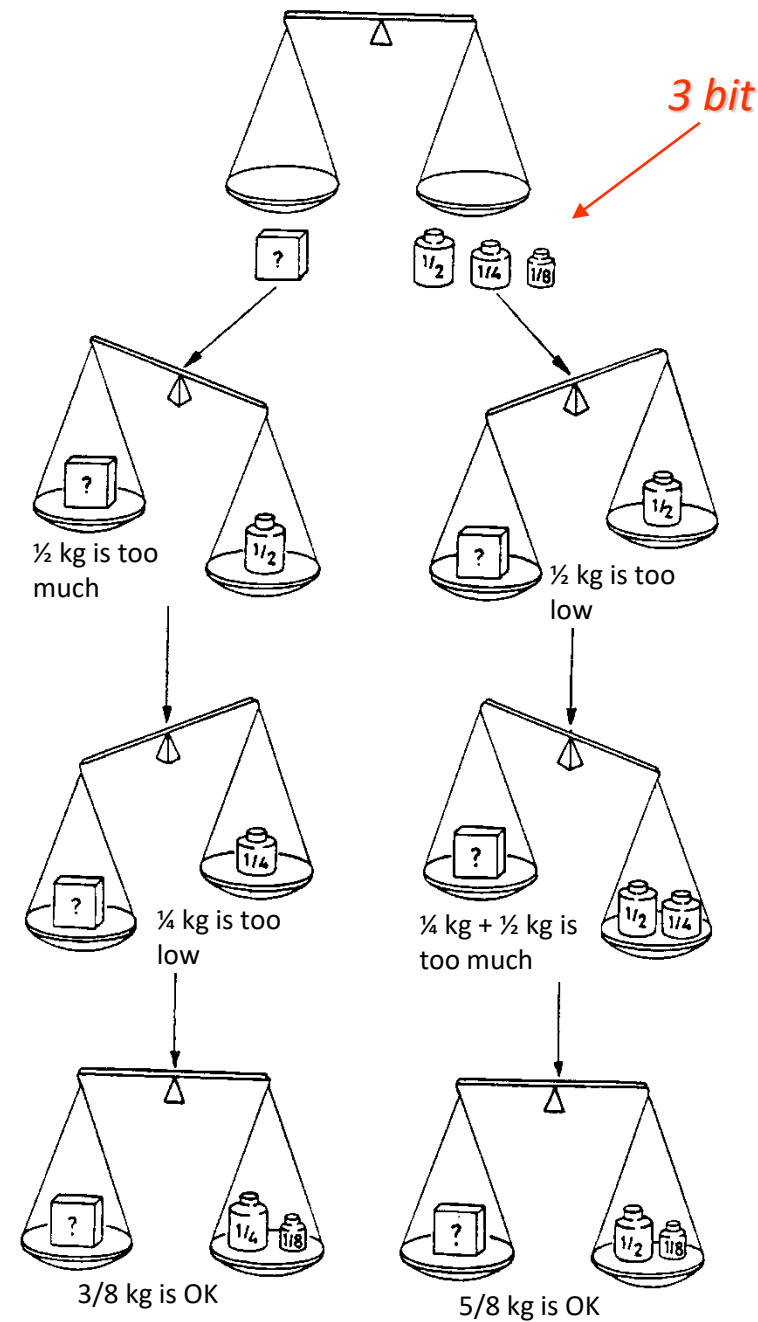
The time t_m is measured by the digital counter, starting when the logic unit connects the internal reference signal and stopping when the “comparator signals to the logic unit” the integrator output v_o has crossed zero !

High resolution (sensitivity) due to the electronic counter / Low frequency of acquisition (around 50 Hz) -
The **sampling period** is at least : $T + t_m$

Successive approximation converter

$011_2 = 3/8 \text{ kg}$
 $1/2\text{kg}=0; 1/4\text{kg}=1; 1/8\text{kg}=1$ (left)

$101_2 = 5/8 \text{ kg}$
 $1/2\text{kg}=1; 1/4\text{kg}=0; 1/8\text{kg}=1$ (right)



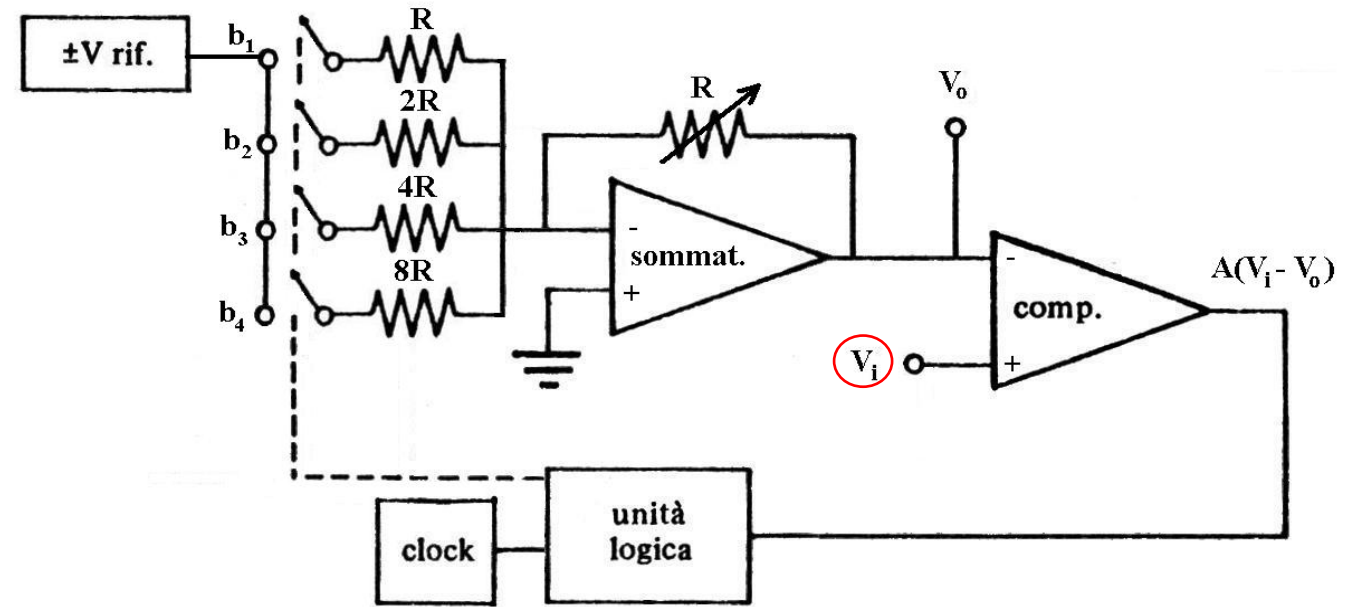
Successive approximation converter

- 1 summing circuit
- 1 comparator
- a reference voltage

This converter is based on the summing Operational Amplifier and the working principle is based on comparing the input signal v_i with “successively added” internal reference voltages.

The logic unit operates successively on the switches b_i with $i = 1, 2, \dots, 4$, which can assume the value **1** (close) or **0** (open).

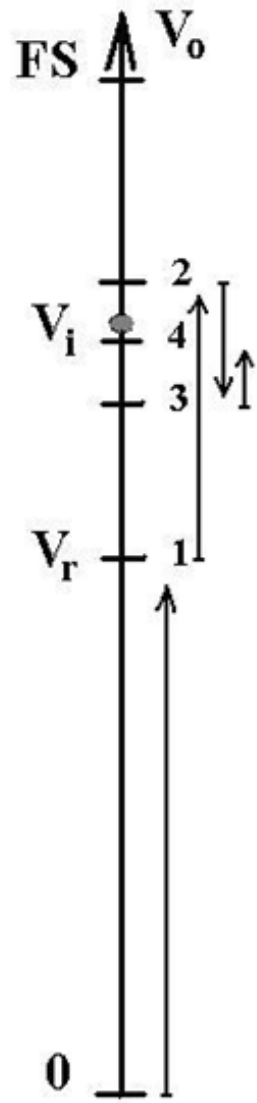
4 bit example



The characteristic curve of the device is therefore:

$$V_o = R \left(\frac{b_1}{R} + \frac{b_2}{2R} + \frac{b_3}{4R} + \frac{b_4}{8R} \right) \cdot V_r = V_r \left(b_1 + \frac{b_2}{2} + \frac{b_3}{4} + \frac{b_4}{8} \right) \frac{R}{R} = V_r \left(b_1 + \frac{b_2}{2} + \frac{b_3}{2^2} + \frac{b_4}{2^3} \right)$$

The procedure goes step by step, as in the next example :



The input unknown signal to the device is V_i : at the beginning all the switches are open

the characteristic curve is : $V_o = V_r \left(b_1 + \frac{b_2}{2} + \frac{b_3}{2^2} + \frac{b_4}{2^3} \right)$

the logic unit closes b_1 : it results

the switch *remains close*: $b_1 = 1$

the logic unit closes b_2 : it results

$V_i > V_1$ the switch *will be reopened*: $b_2 = 0$

the logic unit closes b_3 : it results

$V_i < V_2$ the switch *remains close*: $b_3 = 1$

the logic unit closes b_4 : it results

$V_i > V_3$ the switch *remains close*: $b_4 = 1$

$V_i > V_4$

where V_k $k = 1...4$ is the summing OA output voltage at each step.

At the end of the “successive approximations” procedure we get :

$V_o = V_4 = V_r \left(1 + \frac{0}{2} + \frac{1}{2^2} + \frac{1}{2^3} \right) = \frac{11}{8} V_r$ and the corresponding **binary code** is “1 0 1 1”

Note that the last step $V_o = V_4 \neq V_i$! There is a **discretization error** $\mathcal{E}_d = V_i - V_4$

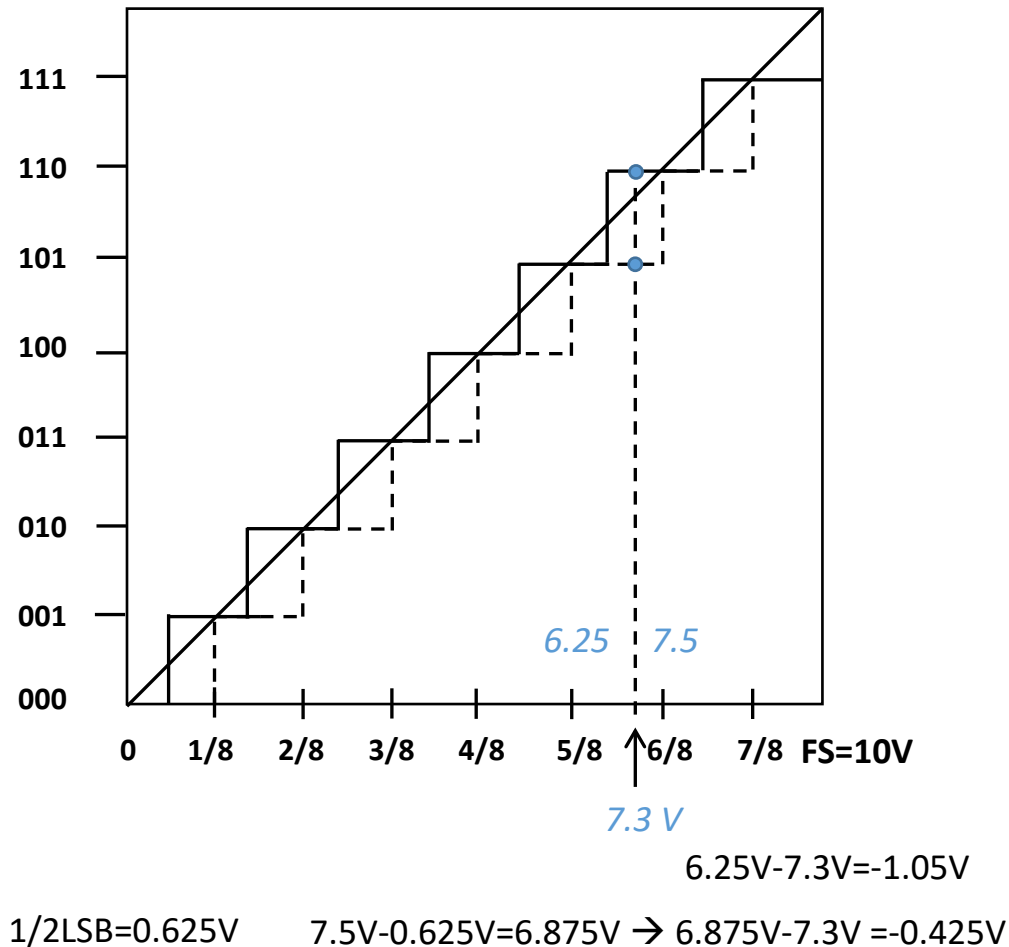
The *discretization error* is due to the *limited number of switches (bits)* of the A/D

converter, in fact the **resolution** of the device is equal to the LSB : $V_{FS} / 2^4 = 2V_r / 16$

Discretization error can be minimized only *adding more bits* (switches) to the A/D converter !

Modern A/D converter have at least *12 bits* or *16 bits*, which means $2^{16} - 1 = 65.536$ discretization levels !

Note also that *successive approximation converters* always approximate by defect the analog value, and to mitigate this problem the characteristic curve is shifted ½ LSB to the left, as shown below for a 3 bit converter :



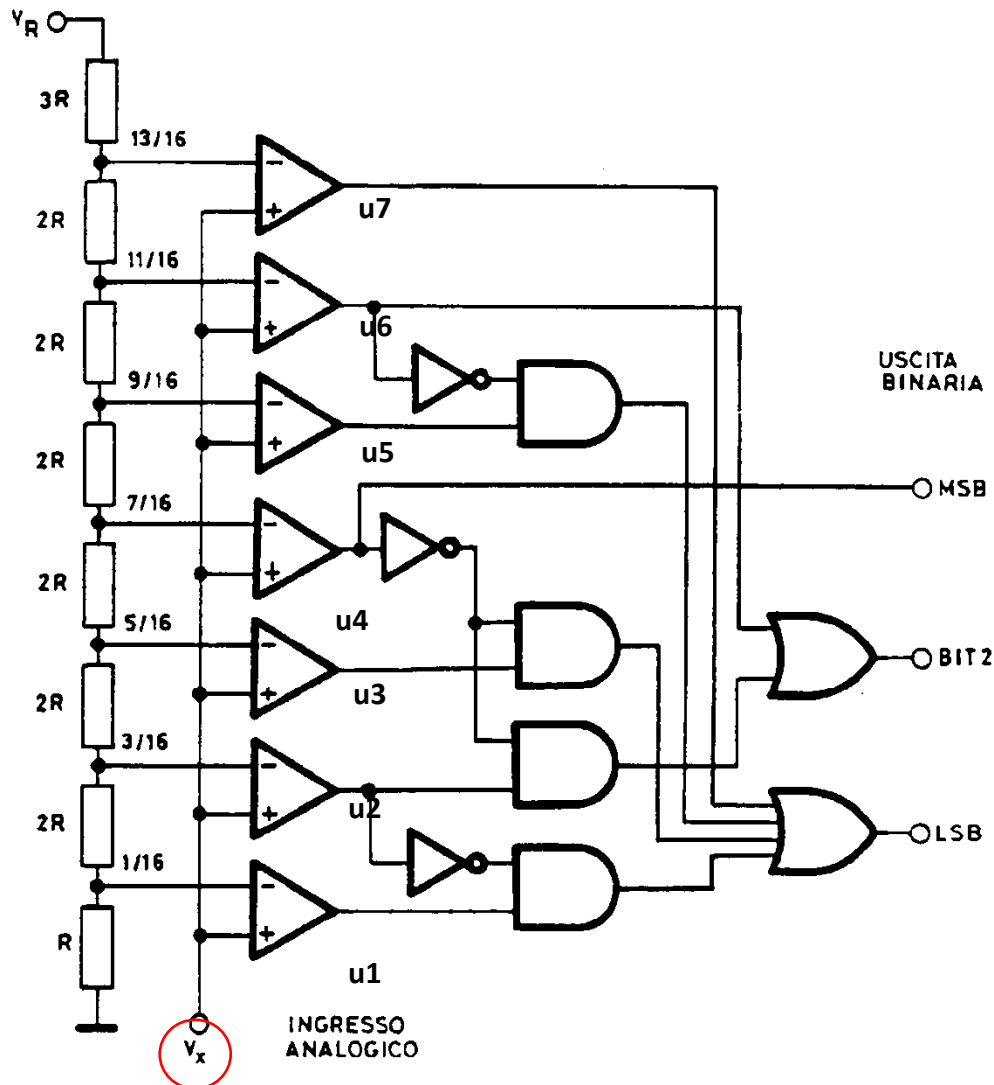
The figure show also another unavoidable error the A/D converters do, the saturation error : when all the bits (switches) are set to 1 the approximated output value is 7/8 of the Full Scale voltage or range : $V_{FS} = 2V_{ref}$.

This problem can be solved only by *increasing the range* of the A/D converter !

Successive approximation A/D converters have a fixed machine time to do the conversion therefore, the sampling period is dependent only on the number of successive approximations (*bits*) and is relatively short (a few μs), which makes this A/D converter a relatively fast device !

The *fastest A/D converter* employed in measurement instrumentation is the **FLASH converter**:

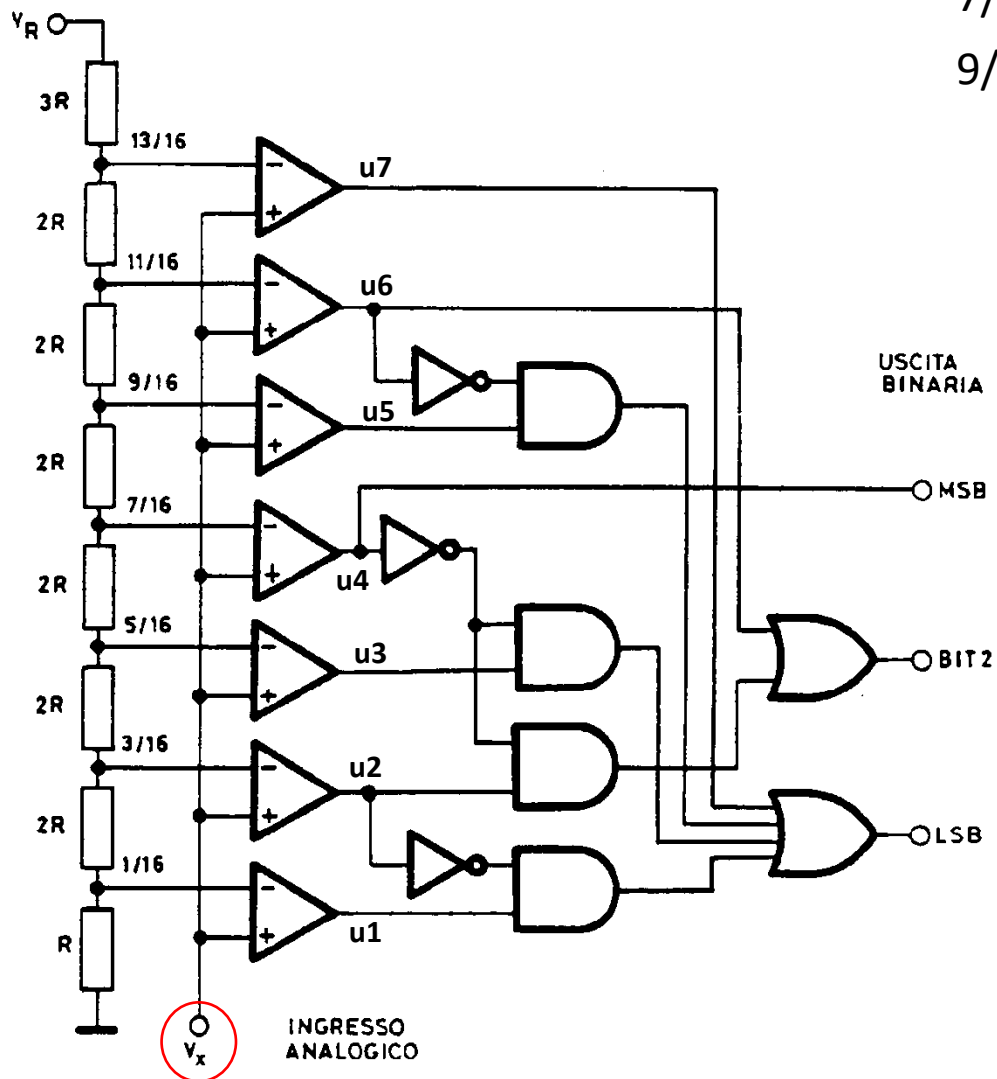
- $2^n - 1$ comparators
- 2^n resistors



The resistor network operates a “voltage partition” from the *full range* V_r to *zero*. The comparators put to 0 (**low**) the output if the input signal V_i is lower than the partitioned inner reference voltage, or to 1 (**high**) if the input signal V_i is higher than the corresponding partitioned voltage !

The comparators work in parallel and do the comparisons all together. The codifying network reconstructs the binary code for the corresponding *input voltage level* !

Flash comparators are *incredibly fast* ($T_c < 1 \mu s$) but are increasingly complicate when the bits increase: an 8 bit comparator requires $2^8 - 1 = 255$ comparators inside.



$$7/16 = 0.4375$$

$$9/16 = 0.5625$$

Eg. $V_x = 0,45V_R$

Then $V_x > 1/16, 3/16, 5/16, 7/16 V_R$

But $V_x < 9/16 V_R$

→ First 4 comparators stay high

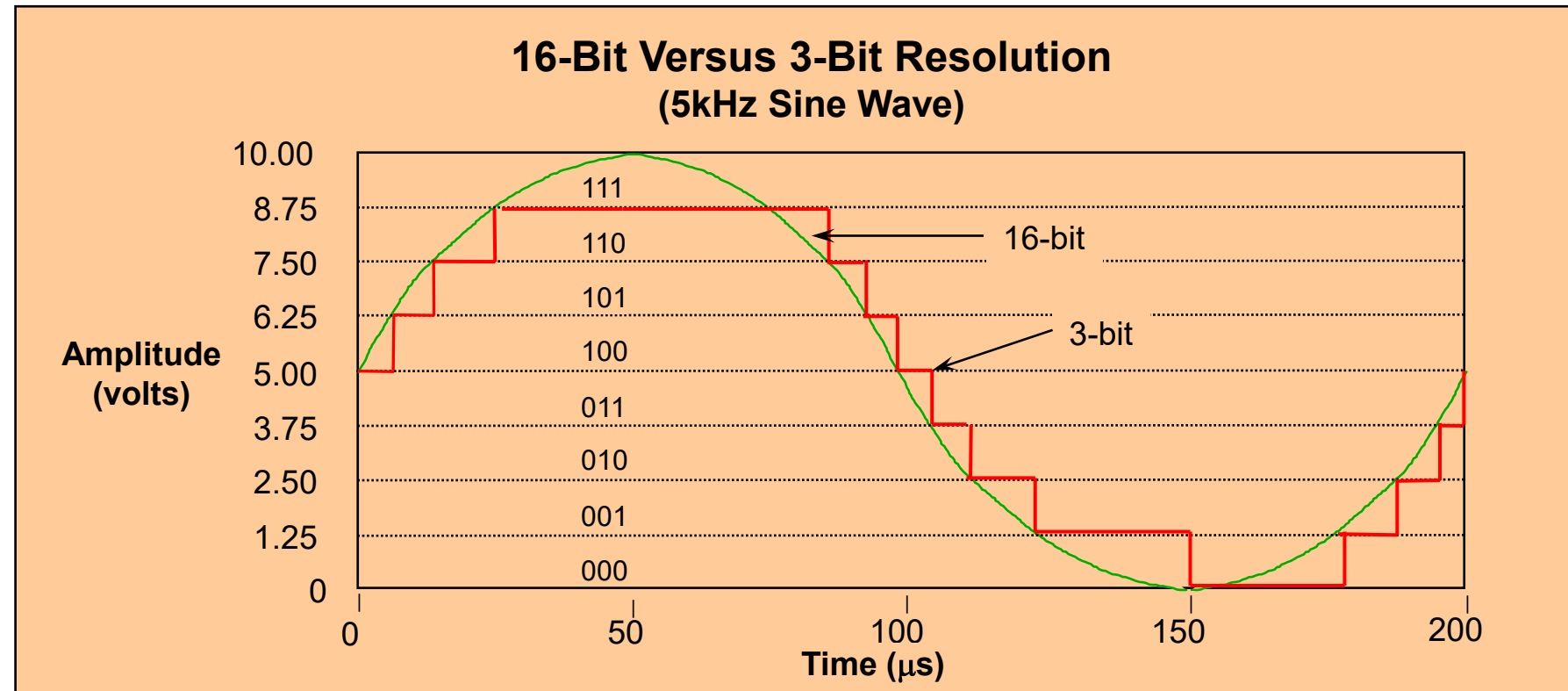
The comparators give in output: 0001111.

This is a digital output but needs to be decoded into a "3-bit" binary output

U7	U6	U5	U4	U3	U2	U1	Binary output
0	0	0	0	0	0	0	0 0 0
0	0	0	0	0	0	1	0 0 1
0	0	0	0	0	1	1	0 1 0
0	0	0	0	1	1	1	0 1 1
0	0	0	1	1	1	1	1 0 0
0	0	1	1	1	1	1	1 0 1
0	1	1	1	1	1	1	1 1 0
1	1	1	1	1	1	1	1 1 1

AD converter resolution

3 bit : $2^3 = 8$
16 bit : 65536



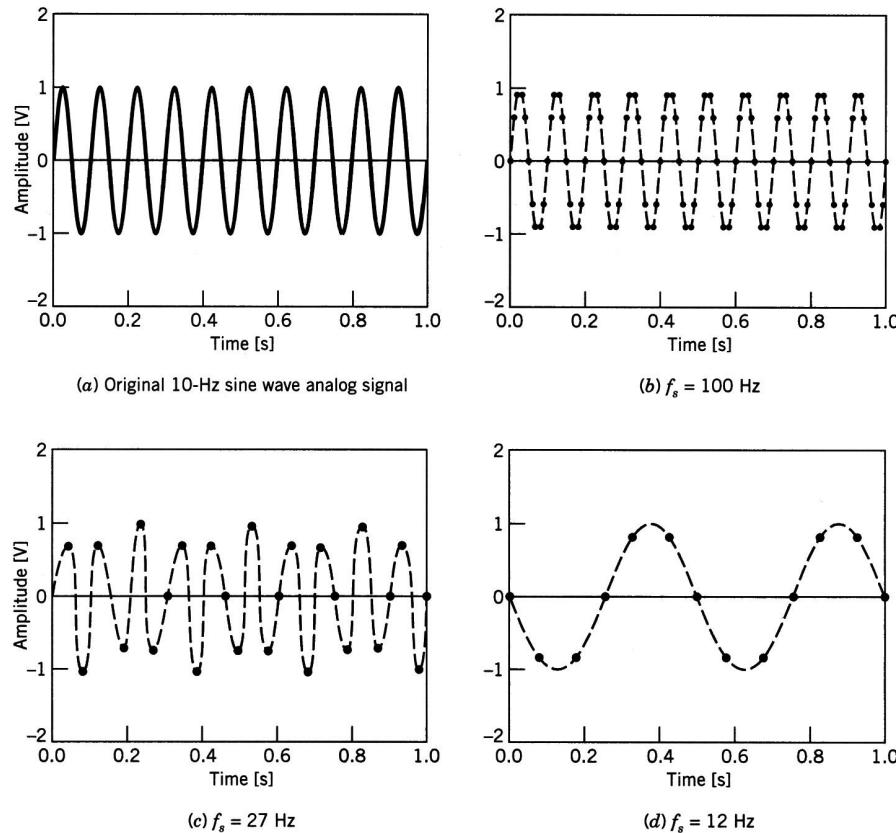
0-10 V input range → ~150 μV

The *velocity of conversion* is directly related to the **dynamic response** of such devices :

If the conversion procedure is fast, the sampling period T_s can be short and the sampling frequency f_s can be high!

The **Nyquist sampling theorem** states that the *sampling frequency of the A/D converter must be at least double of the highest frequency of the signal* : $f_s \geq 2f_{Max}$

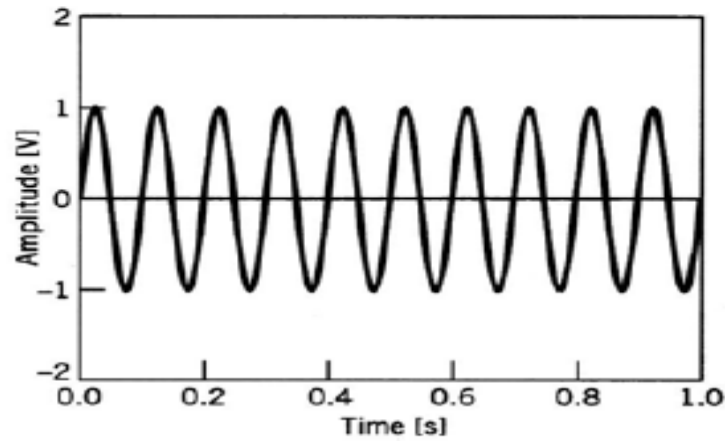
If this rule is not observed, the *discrete signal* will be affected by **aliasing**:



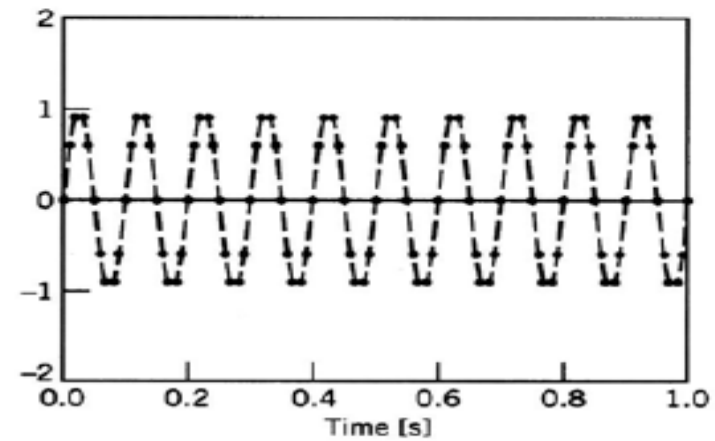
The effect of sample rate on signal frequency and amplitude interpretation.

Be advised that, to have a good digital reconstruction of the analog waveform, it is good practice to use a sampling frequency at least 10 times higher than the signal highest frequency !

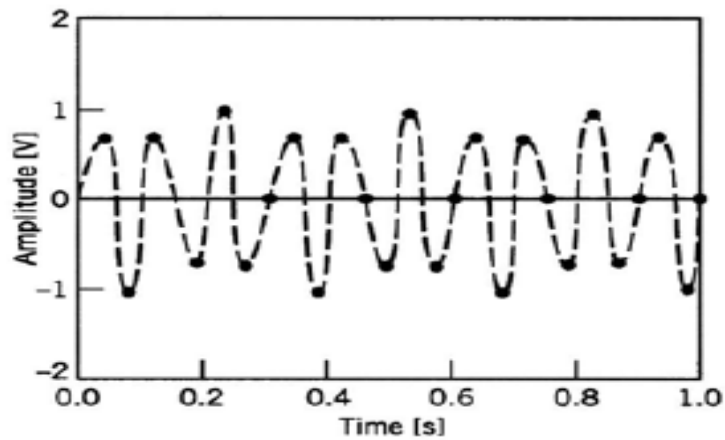
$$f_s \geq 10f_{Max}$$



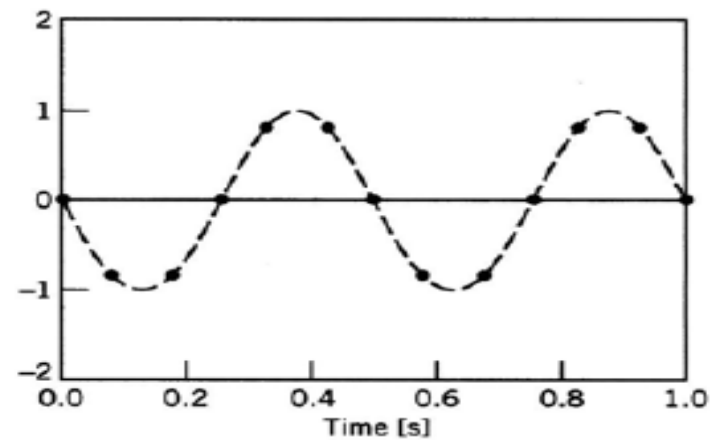
Original 10 Hz sine wave signal



$f_c = 100 \text{ Hz}$

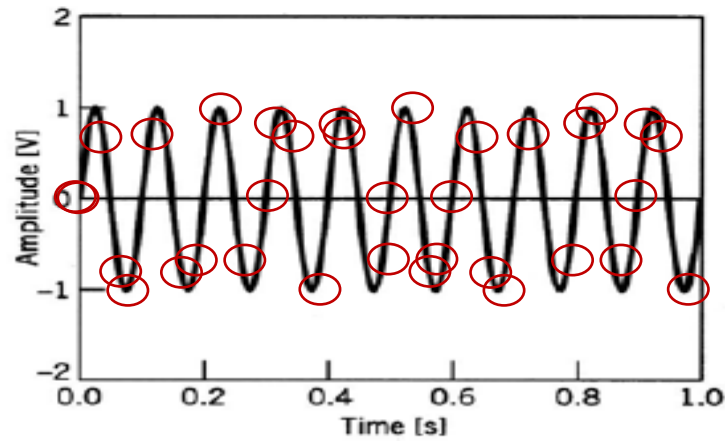


$f_c = 27 \text{ Hz}$

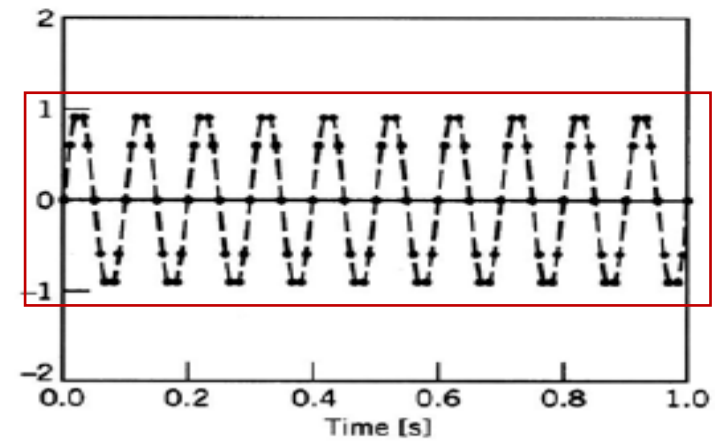


$f_c = 12 \text{ Hz}$

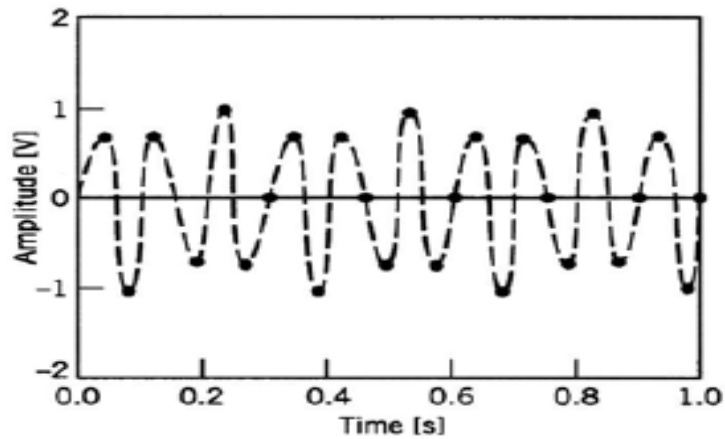
The effect of sample rate on signal frequency and amplitude interpretation.



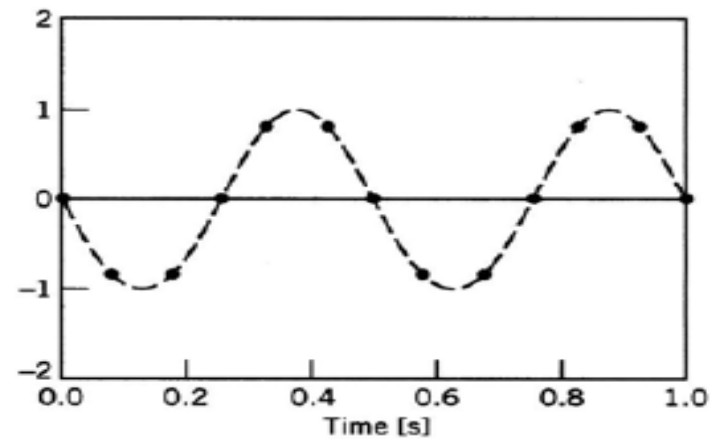
Original 10 Hz sine wave signal



$f_c = 100 \text{ Hz}$



$f_c = 27 \text{ Hz}$



$f_c = 12 \text{ Hz}$

The effect of sample rate on signal frequency and amplitude interpretation.

Example

- Input signal = 0 - 5 Volts
- ADC Range = 0 - 10 Volts
- Gain = 2

